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A 1-5Ghz, Hybrid Mic Wideband LNA utilizing Microstrip Geometric Structure Variety for Performance Improvement

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ABSTRACT

A wideband LNA is design and developed utilizing Hybrid Microwave Integrated Circuit (HMIC) technology for the 1-5GHz bandwidth employing the microstrip line geometric variation. For the performance enhancements in the LNA as for Gain, Noise figure and return loss attributes novel procedures are utilized. The circuit is designed using both lumped elements and distributed components and simulated in AWR microwave office.

The LNA design include optimum biasing circuit and microstrip geometric varieties with two distinct renditioned versions. The first version as the geometric structure with radial stubs and second one as linear stubs and whose basic changes were given in the simulation measurements. This paper likewise gives the reasonable strides in insights with respect to hardware implementations. The proposed design especially helpful in the communication systems working under IEEE L and S bands applications. To be more particular it is having more prominent degree application in the radars and defense receiver systems.

Keywords: LNA, Microwave, Microstrip Lines, biasing Circuit and HMIC.

1 Introduction

Expanding interest to associate more devices wirelessly with higher data rates pushes the industry to adjust new models and send new frequency groups [1]. For the most part all the advanced electronic gadgets, for example, mobiles, portable PCs conceive wireless applications and wireless standards. Each wireless application needs its own front end [2, 3]. A wideband receiver design ought to have the capacity to get an extensive variety of frequency guidelines. This imperative is popular in light of the fact that it grants to diminish the chip region, spare expenses and decrease the RF front-end multifaceted nature [4,9].

Significant requirements on a wideband LNA are to give wideband input matching, high gain with flatness, low NF and adequately high linearity over a vast band of frequencies while keeping power utilization low. The linearity decides how much tolerant is the LNA towards possible solid meddling blockers in the range [11-13].

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2 Collected Research Background

This segment portrays the work in late related s which gives the reasonable support to comprehend what is required to be done to achieve the objectives. D. Bierbuesse,. et.al [5], composed the wideband LNA utilizing all the noise cancellation and a linearization method is exhibited. The outlined LNA comprises of a cross-coupled common-gate topology for wideband matching and noise cancellation. The LNA is planned in a 130 nm CMOS innovation. It has a simulated gain of 14 dB in the frequency run from 100 MHz to 4.7 GHz. The NF is between 3 dB and 4 dB over this frequency band. H. Cruz, et.al [6], presents a wide band LNA for the IEEE 802.11 WLAN. The LNA utilizes two input ways to improve linearity and in-band gain increased. The - 3dB BW is 4 GHz with focus recurrence of 4.7 GHz. The current reuse strategy is used to lessen the power utilization and the NF. Post-Layout design comes about show that the achievable IIP3 is - 2 dBm, and the NF breaks even with 3.07 dB. Peigen Zhou,et.al [7] displayed the outline and usage of a scaled down ultra-wideband LNA reasonable for RF framework. The LNA depends on negative feedback topology and lessens the measure of the circuit enormously. By utilizing a 4.7 Ω resistance in arrangement with the deplete of every transistor, the design output excellent stability at a wideband frequency. The LNA is created on a Rogers RO4003C board with size of 91.5mm*25mm. Over the wide working recurrence band of 2-10GHz, the deliberate outcomes show an astounding execution with the gain of higher than 34dB, in-band evenness of under 3.37dB, S11 of not as much as - 10.95dB, S22 of not as much as - 11.04dB, a low NF of under 3.49dB and a low power utilization. X. Zhang et.al, [8] the proposed LNA indicates enhanced execution parameters including Gain, NF, 1dB P1dB, and information alluded IIP3, especially for wideband LNA outline. The LNA is manufactured in TSMC 0.13-gm prepare. From 0.3 to 6GHz, demonstrate a high-Gain of 20 dB, a predominant NF of 1.6dB at 3GHz, input control at P1dB of - 19.2dBm at 2GHz.

3 The Proposed LNA Design

3.1 The Proposed design flow

This design flow will explore the design parameters space of integrated inductively-low noise amplifiers (LNA), under the constraint of matched input impedance, is presented. It is based on AWR microwave simulation tool and can be easily automated. The approach of the design is shown clearly with details in the flow diagram figure 1 will explore the design parameter space of integrated low noise amplifiers (LNA), under the constraint of matched input impedance.

3.2 The Proposed LNA Design

The design of microwave wideband low noise amplifier operating from 1-5GHz uses Enhancement Mode Psuedomorphic HEMT "ATF54143" 4V and 80mA from Avago Technologies. Lumped elements are used to implement the matching networks. The 2-stage configuration provides required gain. Input and output matching networks are designed to produce 50Ω impedance for maximum power transfer. The achieved specifications are variable gain 17 dB to 30dB, noise figure (NF) of <2dB throughout the band 1 -5GHz, with very good return loss and unconditionally stable condition.

The above figure 2 is the entire schematic diagram of the proposed design of the wideband LNA. It has obviously indicated schematic comprises of the sub block which is having name (net) from left side to be specific "Input Matching Stubs", “Total Ckt”, MLIN, Capacitor and MTRACE2, “Total Ckt” and “Output

Matching Stubs". Every last square will be examined obviously one by one with schematic and designs. The reason, limit and capacity of every sub-square will be examined and analyzed in detail advance.

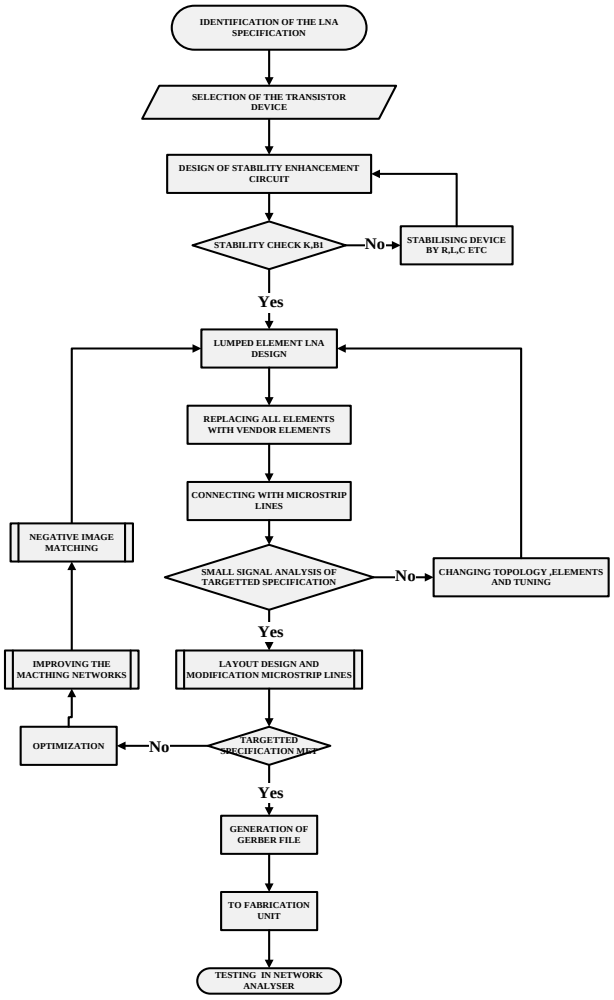


Figure 1 Shows complete work and methodology followed in design of the LNA.

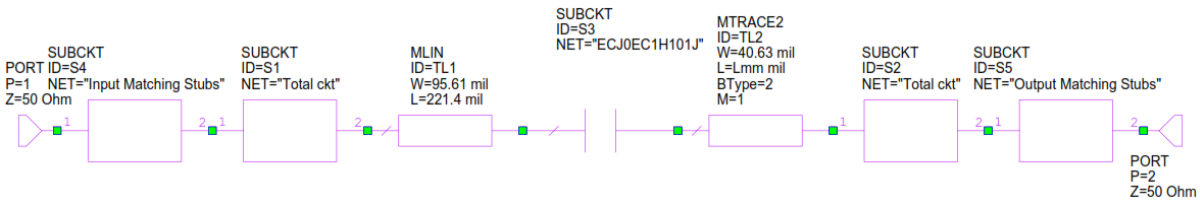


Figure 2 The proposed LNA design Schematic in block form

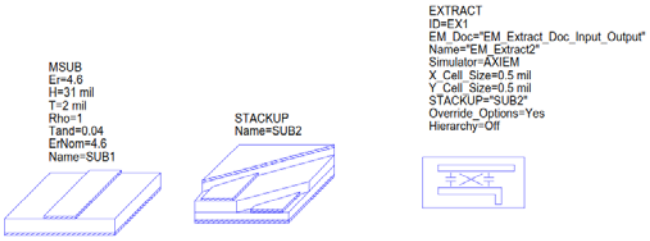


Figure 3 Shows the substrate MODEL, STACKUP AND EXTRACT used in the design

In the figure 3 the square called "MSUB" is utilized to characterize the miniaturized micro strip line in the general circuit design. Er is the permittivity of the substrate material with respect to the permittivity of free space ω0 = 8.85e-12 F/M2, ErNom speaks to the ostensible dielectric steady of the substrate in respect to free space and is utilized just by X-Models where all EM information is gathered at Er_Nom and a variationally approach is utilized to assess the execution for little varieties in Er about Er_Nom or in general nominal dielectric constant. Tand is the dielectric loss digression of the substrate material: Tand = $\varepsilon r'' / \varepsilon r'$ where $\varepsilon r = \varepsilon r' - j \varepsilon r''$, Rho is the mass resistivity of channel metal standardized to gold (that is, to 2.44 x 10 - 8 ω *m). So, real metal mass resistivity = 2.44 x 10 - 8Ω*Rho*m. H and T are cross sectional dimensional factors given in default length units.

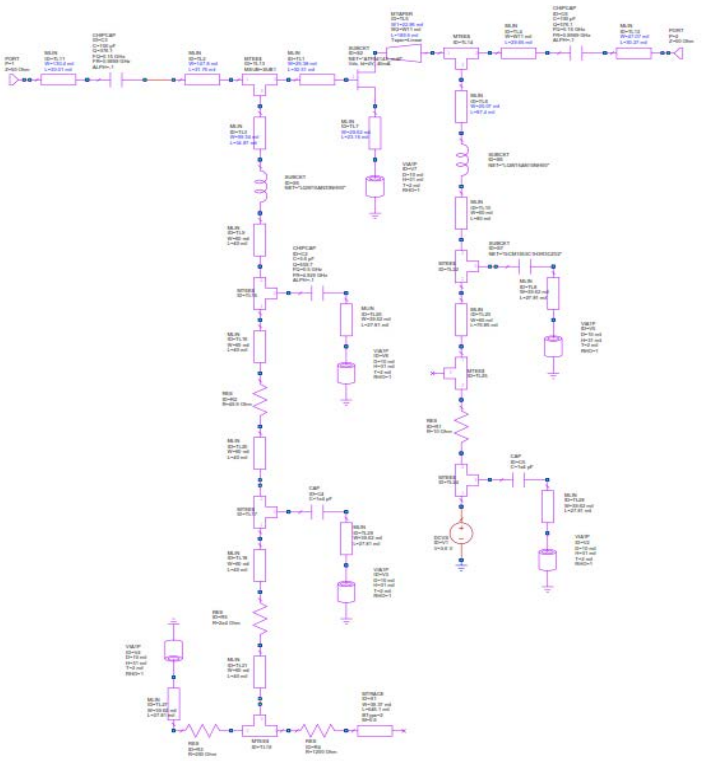


Figure 4 Shows the Sub Block "Total Ckt" of the complete schematic in detail

The sub square "STACKUP" is the Element Options-(Schematic) STACKUP Properties discourse box Material definition which permits to add new materials to structures, determine their properties, and alter and erase these layers. The Conductor and Impedance Definitions characterize the electrical properties of a conduit. For Conductor Definitions, which indicate the conductivity and after that the thickness is determined to the Materials tab. For Impedance Definitions, the thickness is as of now represented in the qualities entered (ohms/sqr). There are two strategies, as now and again you know your material conductivity (gold, copper, and so forth) and now and then it is known dielectric material's impedance (thin film resistors, and so on) [14-16]. The accompanying names are held and can't be utilized: Air, Perfect Conductor, Approx Open, and Input waveguide. It can't include things with these names.

In the figure 3 the sub piece called EXTRACT square is a simulation control that permits a gathering of related schematic components to be electrically displayed by means of a physical reproduction (EM

simulation, parasitic extraction, and so forth.) of the format of these segments. After reproducing, the design cells of the majority of the related segments are ported to an EM sight and simulation. After this reproduction is finished the electrical results are naturally converged once more into the schematic and simulation of the whole schematic is performed.

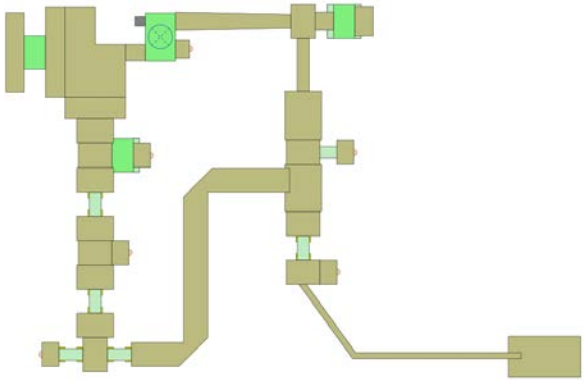


Figure 5 The 2D layout of the sub block "Total Ckt"

The above figure 5 is the sub block of the main circuit schematic figure 2. In order to make cascaded LNA is it good practices by the designer to make first single stage LNA circuit and then followed by that same circuit will be duplicated and connected in series side by side. The cascaded 2 stage amplifier will be done by using 2 "Total Ckt" with intermediate matching by using capacitor "ID S3", "MLIN" and "MTRACE2" which is shown in figure 2. LNA parameters are mainly depend on S parameters which varies with respect to frequency. Also Γin depends on Zin and ΓL, ΓL depends on ZL and ΓIN . Zin and ZL will be different for different biasing components. Effects of biasing components is also frequency dependent

The above figure 5 which is the layout formed for the single stage LNA "Total Ckt". The layout id formed by taking foot prints of each components from the vendors and it is connected by using the micro strip lines. After that high impedance line with patch for soldering the biasing input.

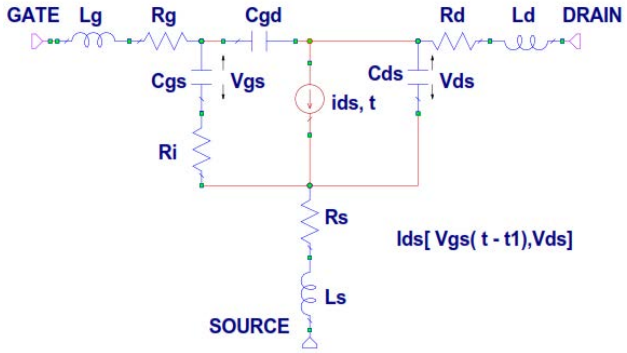


Figure 6 The small signal model of a pHEMT

Cgs and Cgd depends on the biasing voltage because the depletion region changes with the bias.

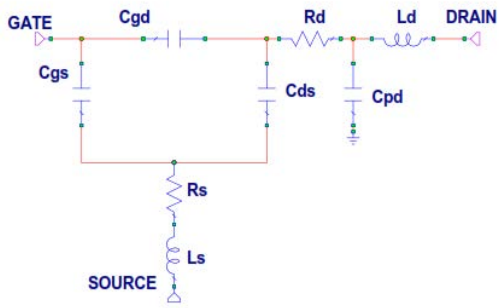


Figure 7 The small signal model of a pHEMT at zero drain bias and gate voltage below pinch-off

The three capacitances Cg, Cs and Cd are given by triangle-star transformation as given below

$$C_g = C_{gs} + C_{gd} + [(C_{gs} * C_{gd})/ C_{ds}] \quad (1)$$

$$C_s = C_{gs} + C_{ds} + [(C_{gs} * C_{ds})/ C_{gd}] \quad (2)$$

$$C_d = C_{ds} + C_{gd} + [(C_{gd} * C_{ds})/ C_{gs}] \quad (3)$$

Input port and output port impedances can be expressed using

$Z_{11} = R_g + R_s + j * [\omega(L_g + L_s) - (1/ \omega) \{ (1/C_g)+ (1/C_s)\}]$ (4)

$Z_{22} = R_d + R_s + j * [\omega(L_d + L_s) - (1/ \omega) \{ (1/C_d)+ (1/C_s)\}]$ (5)

Input reflection coefficient and output reflection coefficient

$$\Gamma_{in} = (Z_{in} - Z_0)/(Z_{in} + Z_0) \quad (6)$$

$$\Gamma_L = (Z_L - Z_0)/(Z_L + Z_0) \quad (7)$$

Equivalent input and output impedances can be expressed in terms of two port Z parameters.

$$Z_{in} = Z_{11} - [(Z_{12} * Z_{21})/(Z_L + Z_{22})] \quad (8)$$

$$Z_L = Z_{22} - [(Z_{12} * Z_{21})/(Z_G + Z_{11})] \quad (9)$$

On the premise of the above arrangement numerical conditions unmistakably reliance of Γin and ΓL furthermore Zin and ZL on Cg, Cs and Cd which changes because of progress in biasing conditions. For the effective outcome, even after fabrication implementations this proposed configuration will be conveyed into two unique forms of the micro strip lines structure.

4 Microstrip Variant Design versions

4.1 Version

This version is done by using negative image matching techniques for the same circuit which is show figure 8. The input matching stubs is prepared for optimizing the input return loss and corresponding gain flatness. The schematic is shown in figure 6.7 and corresponding layout in figure 6.8.

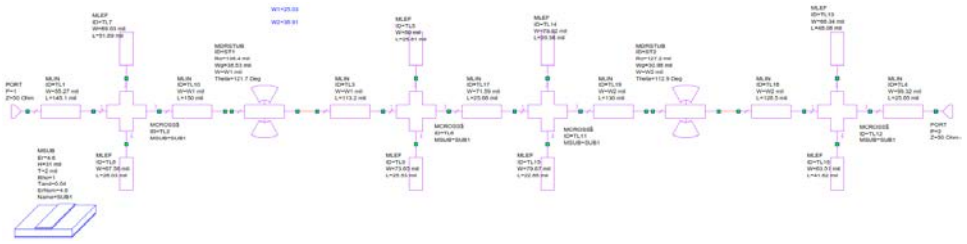


Figure 8 Shows the schematic of the sub block "Input Matching Stubs" of the version 1

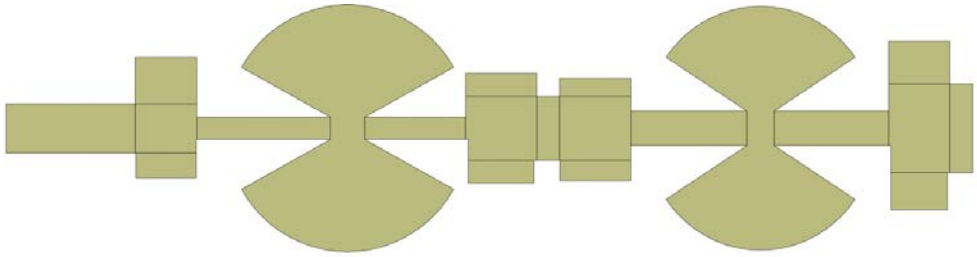


Figure 9 Shows the layout of the sub block "Input Matching Stubs" of the version 1

It is clearly visible that the circuit is prepared by using the micro strip lines structures like "MLIN", "MCROSS", "MLEF" and "MDRSTUB" which means in turn it is linear line, four port junctions, open stub line and radial stubs.

4.1.1 Output Matching Stubs

In this version, output micro strip matching is done by using negative image matching techniques for the same circuit which is shown in figure 2. The input matching stubs is prepared for optimizing the input return loss and corresponding gain flatness. The schematic is shown in figure 10 and corresponding layout in figure 11.

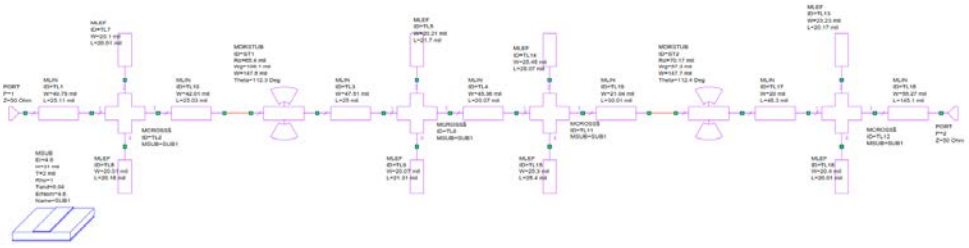


Figure 10 Shows the schematic of the sub block "Output Matching Stubs" of the version 1

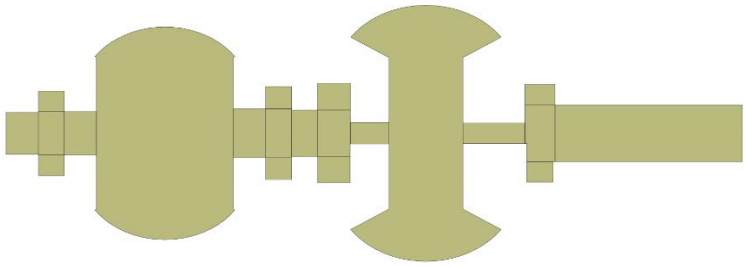


Figure 11 Shows the layout of the sub block "Output Matching Stubs" of the version 1

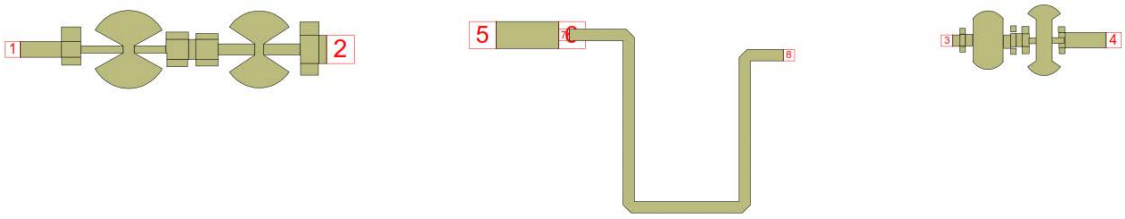


Figure 12 EM Structure circuit for the version 1 circuit

Electromagnetic (EM) test systems is done utilize Maxwell's conditions to process the reaction of a structure from its physical geometry the micro strip line with substrate data and stack up. EM simulation are perfect since they can re-enact exceedingly self-assertive structures and still give extremely exact outcomes. Furthermore, EM test systems are not subject to a large portion of the limitations of circuit models since they utilize key conditions to figure the reaction. One confinement of EM test systems is that reproduction time develops exponentially with the extent of the issue, hence it is critical to minimize issue unpredictability to accomplish opportune outcomes.

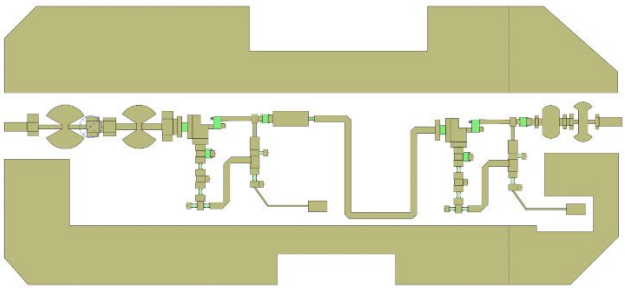


Figure 13 Shows the 2D layout of the complete proposed LNA design version 1

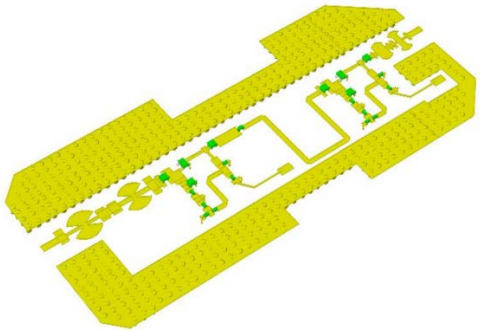


Figure 14 Shows the 3D layout of the complete proposed LNA design version 1

This above figure 13 shows the complete 2D layout and figure 14 shows 3D layout. This is the layout of version 1 changes in input matching stubs and output matching stubs for the complete circuit which has displayed in figure 2. To avoid the parasitic fringing effects the metal outer shape has been provided and series vias are provided to remove or unnecessary charges will be grounded immediately.

4.1.2 Results

The AWRDE features extensive post-processing capabilities, allowing the display of computed data known as "Measurements" on rectangular graphs, polar grids, Smith Charts, histograms, constellation graphs,

tabular graphs, Antenna plots and 3D graphs. There exist an extensive number of the potential electrical and mechanical measurements that are pertinent for the microwave LNA. In any case, there are number of the particulars however all around acknowledged estimations are talked about further.

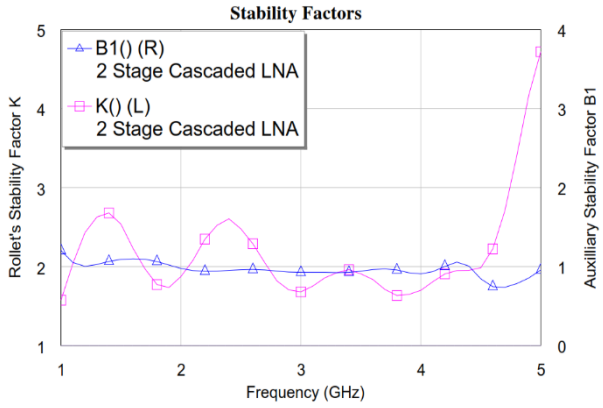


Figure 15 Shows Stability factors: Rollet Factor K and B1 of the proposed LNA design version 1

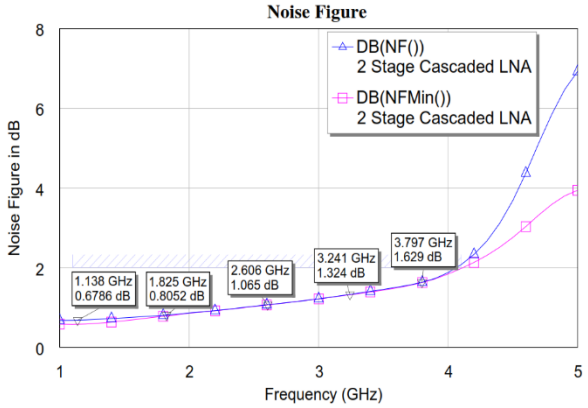


Figure 16 Shows Noise Figure characteristics of the proposed LNA design version 1

The above demonstrated figure 15 shows the stability factors which incorporates Rollet Factors K should greater than 1 and B1 auxiliary factors greater than 0 which is prevailing through the band 1-5GHz. In the figure 16 which is plotted the Noise Figure measurements which is less than 2dB up to 4GHz.

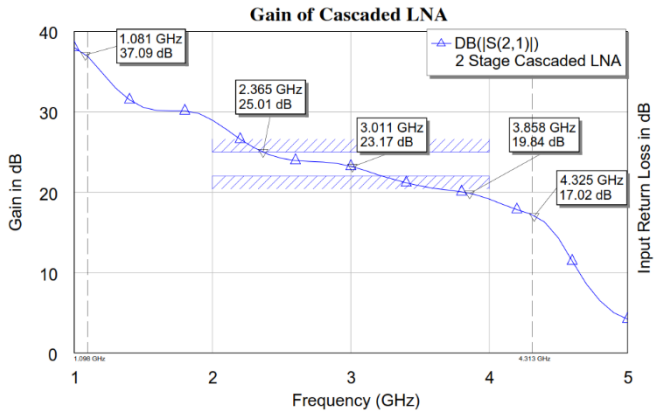


Figure 17 Shows Gain in dB of complete design of the proposed LNA design version 1

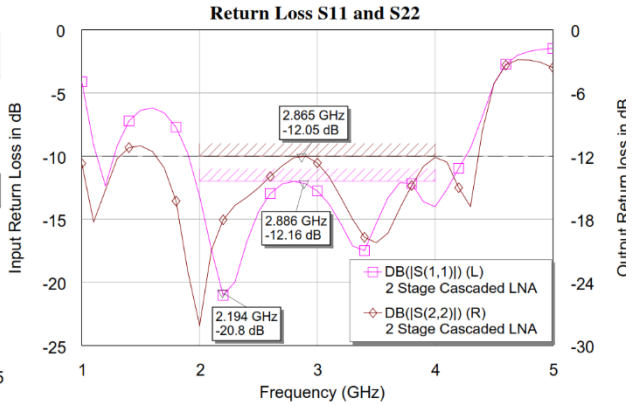


Figure 18 Shows Return loss at both Input and Output Port of the proposed LNA design version 1

In the above figure 17 demonstrates the transducer gain (S21) which is having preferred esteem having more over 20dB up to 4GHz however it is differing from 20dB to 38dB. In the region of the interest between 2-4GHz it is having average of 23dB. Same lines figure 18 shows the very good return loss (S11 and S22) is less than -12dB between 2-4GHz.

4.2 Version 2

This version is done by using negative image matching techniques for the same circuit which is show figure 23. The input matching stubs is prepared for optimizing the input return loss and corresponding gain flatness. The schematic is shown in figure 19 and corresponding layout in figure 20.

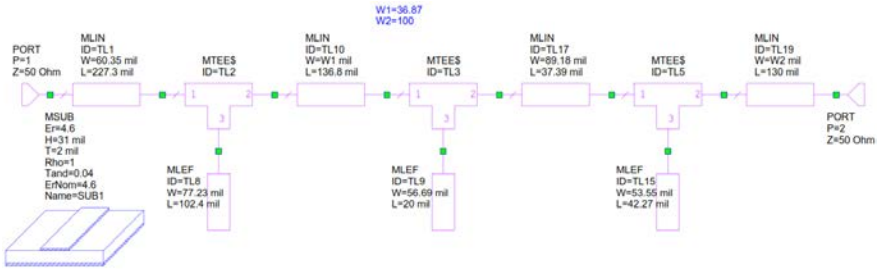


Figure 19 Shows the schematic of the sub block "Input Matching Stubs" of the version 2

4.2.1 Input Match stubs

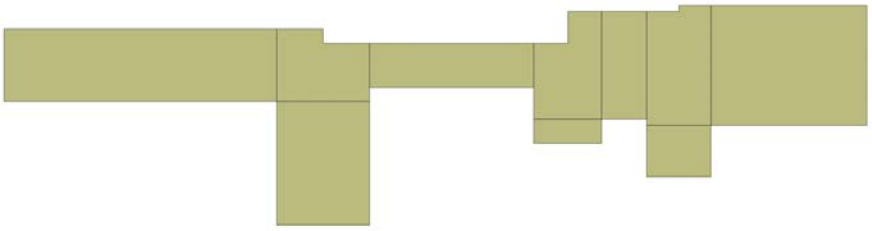


Figure 20 Shows the layout of the sub block "Input Matching Stubs" of the version 2

It is clearly visible that the circuit is prepared by using the micro strip lines structures like "MLIN", "MCROSS", "MLEF" and "MDRSTUB" which means in turn it is linear line, four port junctions, open stub line and radial stubs. In this version, output micro strip matching is done by using negative image matching techniques for the same circuit which is show figure 2. The input matching stubs is prepared for optimizing the input return loss and corresponding gain flatness. The schematic is shown in figure 19 and corresponding layout in figure 20.

4.2.1 Output Match Stubs

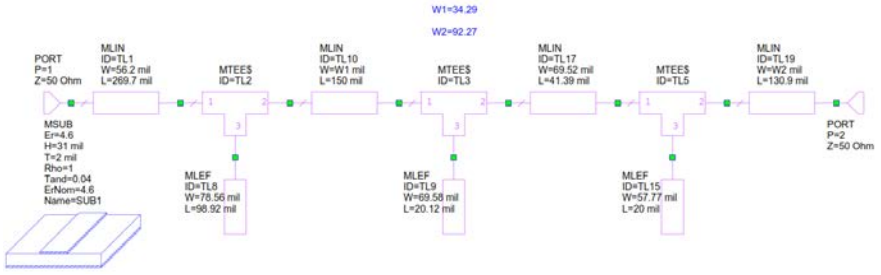


Figure 21 Shows the schematic of the sub block "Output Matching Stubs" of the version 2

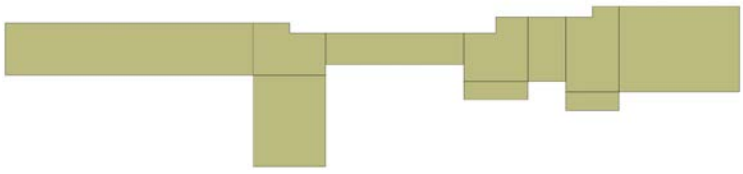
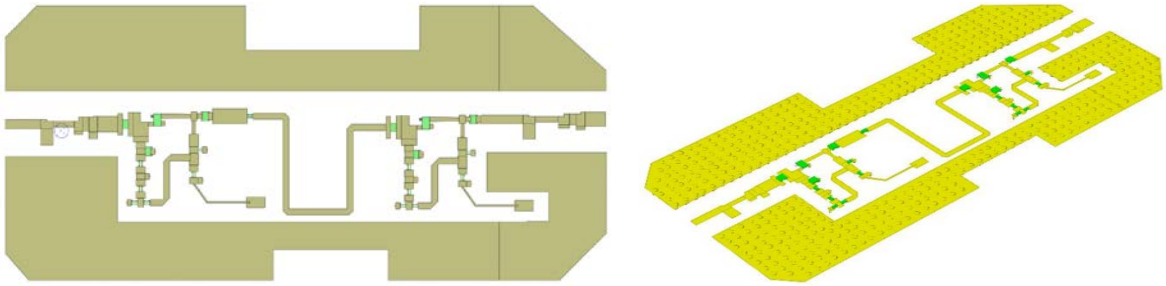


Figure 22 Shows the layout of the sub block "Output Matching Stubs" of the version 2



(a) (b)

Figure 23 Shows the (a) 2D layout (b) 3D layout of the complete proposed LNA design version 2

4.2.2 Results

The AWRDE features extensive post-processing capabilities, allowing the display of computed data known as "Measurements" on rectangular graphs, polar grids, Smith Charts, histograms, constellation graphs, tabular graphs, Antenna plots and 3D graphs.

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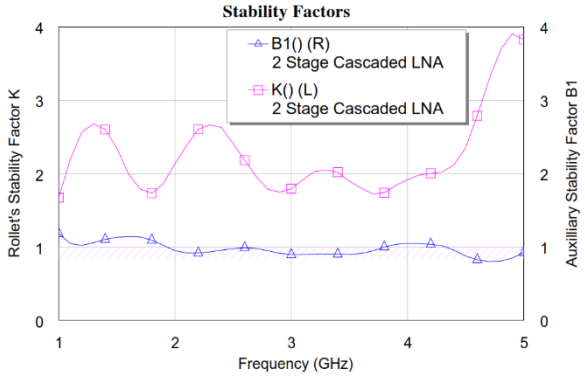


Figure 24 Shows Stability factors: Rollet Factor K and B1 of the proposed LNA design version 2

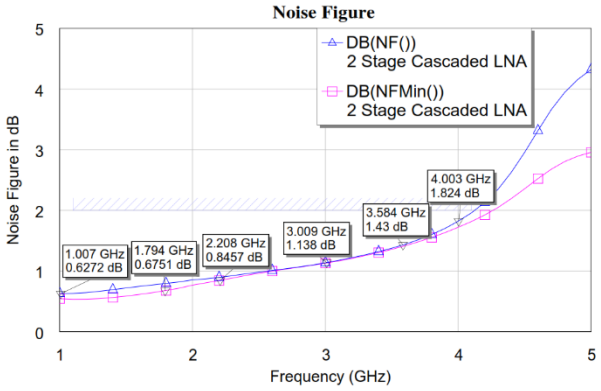


Figure 25 Shows Noise Figure characteristics of the proposed LNA design version 2

The above demonstrated figure 25 shows the stability factors which incorporates Rollet Factors K should greater than 1 and B1 auxiliary factors greater than 0 which is prevailing through the band 1-5GHz. In the figure 26 which is plotted the Noise Figure measurements which is less than 2dB up to 4GHz.

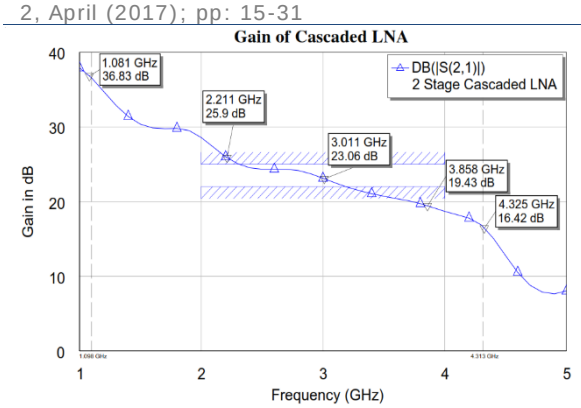


Figure 26 Shows Gain in dB of complete design of the proposed LNA design version 2

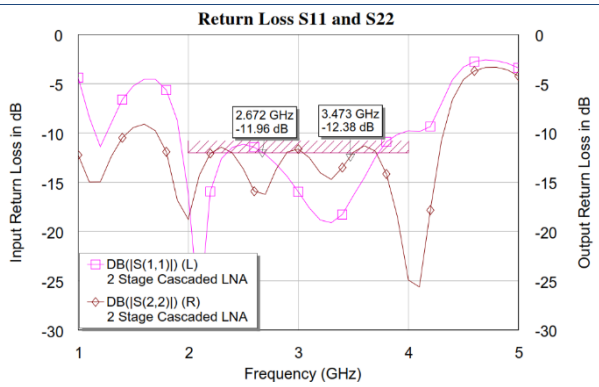


Figure 27 Shows Return loss at both Input and Output Port of the proposed LNA design version 2

In the above figure 27 demonstrates the transducer gain (S21) which is having preferred esteem having more over 20dB up to 4GHz however it is differing from 20dB to 38dB. In the region of the interest between 2-4GHz it is having average of 23dB. Same lines figure 28 shows the very good return loss (S11 and S22) is less than -12dB between 2-4GHz.

5 Theoretical Research Development on the Microstrip Geometric

5.1 Design with Linear Microstrip Line

Figure 29 shows Linear Microstrip Line prototype from AWR tool having length 1600 um width 200 um Port 1and Port 2 are Input and Output Port of Microstrip Line. Layout Design set up by taken care of certain convention. MLIN is used to connect components (Inductor, Capacitor, Transistor), MTEE is used to connect three-point intersection of components and MTAPER is used for smooth tapering between ports by utilising library of AWR Microwave Office Simulation Tool [13]. For transmission power PT from the source and the reflected power PR the return loss in dB as shown in Figure 8 and is given by[4],

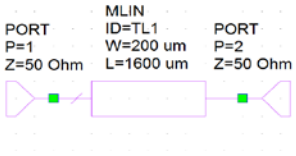


Figure 28 Microstrip Line (MLIN)

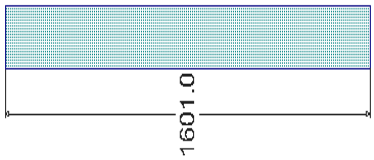


Figure 29 Layout of Microstrip Line (MLIN)

$$RL\ (dB) = 10\ log_{10}\left(\frac{P_T}{P_R}\right) \quad (10)$$

For unconditional stability [14],

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (11)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (12)$$

$$F_{total} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \frac{F_4-1}{G_1G_2G_3} + \ldots \quad (13)$$

where, Fn are the noise factor and Gn are available power gain, individually of the n^{th} phase. Note that both magnitudes need aid communicated as ratios, not clinched alongside decibels

5.2 Design with Mitered (U-bend) Microstrip Line

For Mitering Microstrip Line, Meander Line 2 closed form (MTRACE2) is used instead of Microstrip Line (MLIN) in AWR Microwave Office with Miter Length to Width ratio = 1. Whole Design remains same with same Matching Networks.

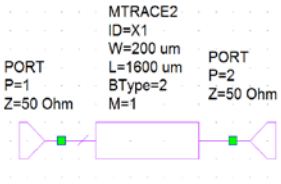


Figure 30 Meander Line 2 closed form (MTRACE2)

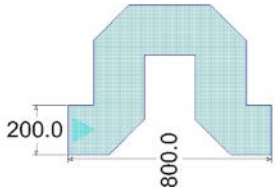
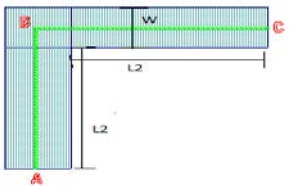
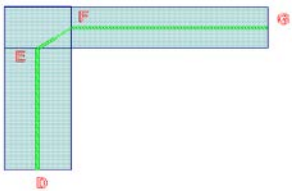


Figure 31 Layout of Meander Line 2 closed form (MTRACE2)



a



b

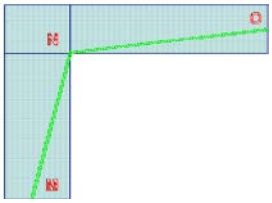
Figure 32 Determination of equivalent length for unmetered right-angled bend. a) Centreline approach. b) Modified centreline approach.

Figure 33.a shows centreline approach and the equivalent length (L_{eq}) is equal to length **ABC** will be given by[12],

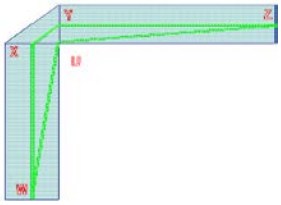
$$L_{eq} = 2L_2 + W \tag{14}$$

Figure 33.b shows Modified centreline approach and the equivalent length (L_{eq}) is equal to length **DEFG** which shows actual current flow will be given by [12],

$$L_{eq} = 2L_2 + \frac{\sqrt{2}}{2} W \tag{15}$$



a



b

Figure 33 Current path approximations. a) Shortest path. b) Shortest path and modified centerline path.

According to figure 34.a, Due to deviation in current density that is high current density at edges and low current density at center of Microstrip Line current path will not follow the centreline path (**ABC**), but deviates towards the shortest path (**MNO**). For the unmitered right-angled bend the corrected current

path by modifying the centreline path, equation (5), into a path following the inner edge more closely (**DEFG**) given by equation (6). The shortest path length, L_{shrt} (**MNO**), follows from figure 34.a,

$$L_{short} = \sqrt{\left(\left(\frac{W}{2}\right)^2 + (L_2)^2\right)} \quad (16)$$

The equivalent length of the 50% mitered right-angled microstrip bend, L_{eqmit2} (**WXYZ**) , is now calculated as[12],

$$L_{eqmit2} = \sqrt{L_{Short} \cdot L_{eq2}} \quad (17)$$

Where, L_{eq2} is given by equation (5).

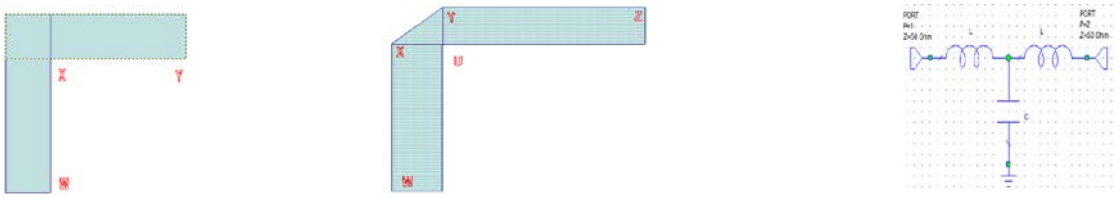
Optimum miter is given by [16],

$$\frac{X}{D} = 0.52 + (0.65 * e^{\left(-1.35*\left(\frac{W}{H}\right)\right)}) \quad (18)$$

Range of Usage,

$0.5 \leq \frac{W}{H} \leq 2.75$ and $2.5 \leq \varepsilon_r \leq 25$

Where, ε_r = dielectric constant (from associated Substrate), H = substrate thickness (from associated Substrate), W = conductor width, in specified units W ≥ 0 for layout



a b c

Figure 34 A) Microstrip corner B) Mitered corner C) Equivalent circuit

The equivalent circuit of a microstrip corner is shown in fig. 35 .a. The values of the components are as follows [11].

$$C\,[pF] = W \cdot [(10.35 * \varepsilon_r + 2.5) * (\frac{W}{h}) + (2.6 * \varepsilon_r + 5.64)] \quad (19)$$

$$L\,[nH] = 220 * h * [1-1.35 * \exp(-0.18 * (\frac{W}{h})^{1.39})] \quad (20)$$

The values for a 50% mitered bend are [11].

$$C\,[pF] = W \cdot [(3.93 * \varepsilon_r + 0.62) * (\frac{W}{h}) + (7.6 * \varepsilon_r + 3.80)] \quad (21)$$

$$L\,[nH] = 440 * h * [1-1.062 * \exp(-0.177 * (\frac{W}{h})^{0.947})] \quad (22)$$

With W constantly width of the Microstrip accordance Furthermore h stature the height of the substrate. The Z-parameters to those provided for proportional little sign out might make composed Similarly as underneath mathematical statement What's more would simple to change over with to scattering parameters [10].

$$Z = \begin{bmatrix} j\omega L + \left(\frac{1}{j\omega C}\right) & \frac{1}{j\omega C} \\ \frac{1}{j\omega C} & j\omega L + \left(\frac{1}{j\omega C}\right) \end{bmatrix} \quad (14)$$

6 Prime novelty Statement

The proposed design of the LNA is carried using negative image matching technique at the input and output of the circuit using microstrip line with two different versions to understand how major parameters of the LNA to be identify, distinguish and characterized. The prime novelty of the research is on biasing technique, negative image matching and Microstrip line geometric structure variations for particular application context. Expecting that LNA design processing problems are resolved and integrating the lumped elements with Microstrip lines using HMIC manufacturing technique.

1. Special Design of LNA which covers the applications of IEEE Bands L and S.

2. Experimented optimum biasing circuits, micro strip lines and variation towards the LNA frequency measurements.

3. Negative Image Matching techniques are applied for both input and output matching circuits.

5. To have good performance with the sensitivity of the circuit, this research provided effect on biasing circuit on the small signal analysis.

The novelty dwells in a unified approach that deals with the interpretation, design, analysis and optimization of the LNA parameters in their mutual relevant requirements to improve the imperatives LNA performance.

7 Conclusion

This research work includes design, measurement, analysis of microwave low noise amplifier over the IEEE frequency bands L and S. Furthermore, investigating of Linearity, Gain, Stability and Return Loss which also demonstrates low noise amplifier schemes to enhance efficiency and linearity by controlling the number of amplifiers parameters in operation. This paper gives clear thought regarding the geometric varieties of the microstrip lines execution as for LNA estimations. In like manner, the design as two renditions versions which is having same design with various microstrip line components model variety.

REFERENCES

[1]. A. Abdelhamid, M. T. Ozgun and H. Dogan, "A highly integrated wideband LNA with multiple inputs for multi-band mobile devices," 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, United Arab Emirates, 2016, pp. 1-4. doi: 10.1109/MWSCAS.2016.7870076.

[2]. A. Pandey, M. Pusalkar and P. Dwaramwar, "A 0.1–3 GHz, 90nm CMOS wideband LNA employing positive negative feedback for gain, NF and linearity improvement," 2016 International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), Ramanathapuram, 2016, pp. 147-152. doi: 10.1109/ICACCCT.2016.7831618.

[3]. M. Pusalkar, A. Pandey and P. Dwaramwar, "A 0.3–3.3GHz low power, low noise figure, high gain inductor-less wideband CMOS LNA," 2016 International Conference on Advanced Communication Control and

Computing Technologies (ICACCCT), Ramanathapuram, 2016, pp. 196-201. doi: 10.1109/ICACCCT.2016.7831629.

[4]. P. Bousseaud, M. A. Khan and R. Negra, "Inductorless wideband LNA with improved input matching using feedforward technique," 2016 46th European Microwave Conference (EuMC), London, 2016, pp. 1027-1030. doi: 10.1109/EuMC.2016.7824521.

[5]. D. Bierbuesse, P. Bousseaud and R. Negra, "Inductorless and cross-coupled wideband LNA with high linearity," 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), Oslo, 2015, pp. 1-4. doi: 10.1109/NORCHIP.2015.7364391.

[6]. H. Cruz, S. Y. Lee and C. H. Luo, "A 3-to-7GHz wideband LNA with IIP3 of −2dBm and 0.5dB in-band gain ripple," 2015 IEEE International Wireless Symposium (IWS 2015), Shenzhen, 2015, pp. 1-4. doi: 10.1109/IEEE-IWS.2015.7164627.

[7]. Peigen Zhou, Daxu Zhang and Jixin Chen, "A 2–10GHz ultra-wideband high gain negative feedback low-noise amplifier," 2016 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT), Beijing, 2016, pp. 58-60. doi: 10.1109/ICMMT.2016.7761676

[8]. X. Zhang, L. Yang and F. Huang, "A 0.3–6GHz broadband noise cancelling low noise amplifier," 2016 International Conference on Integrated Circuits and Microsystems (ICICM), Chengdu, 2016, pp. 144-148. doi: 10.1109/ICAM.2016.7813581

[9]. A. K. Ray and R. C. Shit, "Design of ultra-low noise, wideband low-noise amplifier for highly survival radar receiver," in IET Circuits, Devices & Systems, vol. 10, no. 6, pp. 473-480, 11 2016. doi: 10.1049/iet-cds.2016.0065

[10]. M. Kirschning, R. H. Jansen, and N. H. L. Koster, ``Measurement and Computer-Aided Modeling of Microstrip Discontinuities by an Improved Resonator Method,'' IEEE MTT-S International Microwave Symposium Digest, pp. 495-497, May 1983.

[11]. L. Pantoli, A. Barigelli, G. Leuzzi and F. Vitulli, "Analysis and design of a Q/V-band low-noise amplifier in GaAs-based 0.1 µm pHEMT technology," in IET Microwaves, Antennas & Propagation, vol. 10, no. 14, pp. 1500-1506, 11 19 2016. doi: 10.1049/iet-map.2016.0422

[12]. A. K. Ray and R. C. Shit, "Design of ultra-low noise, wideband low-noise amplifier for highly survival radar receiver," in IET Circuits, Devices & Systems, vol. 10, no. 6, pp. 473-480, 11 2016. doi: 10.1049/iet-cds.2016.0065

[13]. F. Ma, X. W. Zhang and B. Y. Chi, "A 100M–1.5 GHz harmonic-rejection SDR receiver front-end," 2015 IEEE 11th International Conference on ASIC (ASICON), Chengdu, 2015, pp. 1-4. doi: 10.1109/ASICON.2015.7516892

[14]. M. N. Karim and P. K. Saha, "Optimal design of a low power UWB LNA for 5–10 GHz application," 2015 18th International Conference on Computer and Information Technology (ICCIT), Dhaka, 2015, pp. 213-216. doi: 10.1109/ICCITechn.2015.7488070

[15]. B. Adhikari, P. Jain and Jamadagni H. S., "An ultra-wideband frequency Domain receiver for software defined radio applications," 2015 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, 2015, pp. 1-6. doi: 10.1109/CONECCT.2015.7383934

[16]. G. de Streel, D. Flandre, C. Dehollain and D. Bol, "Towards ultra-low-voltage wideband noise-cancelling LNAs in 28nm FDSOI," 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Rohnert Park, CA, 2015, pp. 1-2. doi: 10.1109/S3S.2015.7333487

[17]. L. Ma, Z. Wang, J. Xu and O. Zhang, "A 500 kHz-1.4 GHz push-pull differential noise cancellation LNA," 2015 IEEE International Conference on Communication Software and Networks (ICCSN), Chengdu, 2015, pp. 182-185. doi: 10.1109/ICCSN.2015.7296150

[18]. S. Lee, D. Jeong, H. Jin and B. Kim, "Reconfigurable 4 channel carrier aggregation receiver using harmonic recombination technique," 2016 11th European Microwave Integrated Circuits Conference (EuMIC), London, 2016, pp. 1-4. doi: 10.1109/EuMIC.2016.7777473

[19]. Z. Hong-min, Z. Ying, Y. Ying and D. Ke-ke, "Analysis and design of a 3.1–10.6 GHz wideband low-noise amplifier using resistive feedback," 2016 IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB), Nanjing, 2016, pp. 1-3. doi: 10.1109/ICUWB.2016.7790609

[20]. A. Mattamana, W. Gouty, W. Khalil, P. Watson and V. J. Patel, "Multi-Octave and Frequency-Agile LNAs Covering S-C Band Using 0.25 µm GaN Technology," 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Austin, TX, 2016, pp. 1-5. doi: 10.1109/CSICS.2016.7751057

