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SERVICES FOR SCIENCE AND EDUCATION

Signal Integrity Engineering Redefined: To Include RF Stages Deploying CMOS VLSI Devices and Traces (As in Bluetooth)

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ABSTRACT

This paper revisits the general definition of *signal integrity* (SI) engineering to include relevant considerations applied to RF stages (front- and/or back-end) of wireless system compliant devices such as Bluetooth, ZigBee, mobile phone etc. Apart from traditionally viewed (baseband) impairments specific to digital waveforms, possible artifacts caused by RF-stage electromagnetics that influence the SI undesirably are identified. Hence, SI is redefined more comprehensively to include RF contexts. Relevant ADS™-based simulation results on transmit-receive (TR)-switch performance in a CMOS-VLSI based Bluetooth circuit are presented and discussed.

Keywords: Signal integrity, CMOS VLSI, Submicron RF devices, IEEE 802.11 devices, PCB traces.

INTRODUCTION: WHAT IS SIGNAL INTEGRITY?

Mostly *signal integrity* (SI) in its traditional definition is viewed in a restricted perspective as the net effect of all impairments to a "digital waveform" traversing across the plethora of active devices and passive components in a circuit or a system. Relevant engineering posed thereof is to understand the underlying phenomenon of collective (impairment) effects seen in "real world" circuits and find control/mitigations efforts to maintain a reliable, error-free digital signal transport. within the circuits and/or systems of interest [1].

Thus, conventional SI in essence involves estimating the quality of an electrical signal denoting a stream of binary waveform (in digital format of voltage or current), transported *via* interconnections across devices and components in a circuit and/or a system. Such transports over (electrically) short distances (of interconnections) may remain with sufficient fidelity, especially at low bit rates. However, at high bit rates (and over longer electrical distances), there are effects that can degrade the electrical signal waveform to the extent of mutilation that makes the receiving device either unable to recognize the signal or wrongly interpret it, for example, a waveform assigned to denote logic 0 being registered as logic 1 (or *vice versa*) causing soft-errors. In addition to pulse transit related influences, there are also issues like power transients, electrostatic discharge and electrical overstressing (ESD/EoS) effects as well as ionizing radiation stresses that may lead to soft-error infestation.

Within the purview of classical definition of SI as above, the SI engineering implies the task of analyzing and mitigating the impairments observed in digital signal waveforms at all locales and levels in circuits and systems. Specifically, SI concerns *vis-à-vis* digital waveforms are expressed at: Electronics packaging, connections within an integrated circuit (IC) through the package, on-chip connections, chip-to-chip connections, the printed circuit board (PCB) traces, the backplane layout, and inter-system connections. Mostly the interconnect flight time *versus* the bit period is emphasized in specifying the integrity of such digital waveforms. Some issues of SI thereof pertinent to digital waveforms refer to:

- **Crosstalk**: The crosstalk in VLSI/ULSI configurations (and in densely laid out PCBs) implies transfer of undesirable signal from one line to another due to inevitable electromagnetic (EM) coupling (especially in densely packed traces of lines). Appearance of such spurious signal cross-transferred onto a legitimate signal invariably would cause a 'distortion' in the signal waveform manifesting as delay effects. In modern circuit design technology, because of increasing device density and operation speed, crosstalk effects are almost inevitable between circuit elements [1-3].
- **Ringing**: This is an unwanted oscillation observed in voltage or current waveforms, particularly in an electrical pulse due to the presence of parasitic reactive components (capacitances and inductances) existing in the signal path.
- **Ground bounce**: This refers to a transient voltage generated between two different points on the same ground path, such as a package lead, a connector pin or different locations on the ground plane of a circuit board. In high-density digital circuits, ground bounce implies a delay in reaching ground after a signal transition taking place in a transistor. This means an unstable logic state.
- **Power-supply noise**: The disturbances and fluctuations of the power-supply voltage of internal blocks cause power-supply voltage noise (power transients) leading to gate delay variations.
- **ESD (Electrostatic discharge)/EoS (Electrical overstressing) effects**: The adverse influence of electrostatic discharge and electrical overstressing on MOS devices are well known [4]. The advent of extreme scaling into sub-quarter micron dimensions leads to unique concerns of SI interest.
- **Ionizing radiation stresses** that lead to soft-error infestation [5].

Traditionally, SI engineering defined above is attributed to the exclusive infrastructure of high-speed digital networks where crosstalk considerations are primary issues in maintaining signal integrity, which as defined thereof would include the net effect of all impairments (enumerated above) to a digital waveform as it traverses through various components between active devices in a circuit or a system. Efforts to assess or measure such impairments in digital waveforms (and take proactive mitigation measures to reduce them) constitute the formal theme of conventional signal integrity engineering.

SI-related Issues with Digital Waveforms

As well known, a trace (of interconnection) denotes a transmission-line with a characteristic impedance, $Z_o = (L_o/C_o)^{1/2}$ ohm, where L_o and C_o denote the inductance per unit length (in H/m) and capacitance per unit length (in F/m) of the line respectively. The value of Z_o *versus* the terminal impedance is crucial in deciding the matching (and hence the signal reflection involved). Because of any low impedance situation set by (mis)matching, PCB signal-traces and interconnects may carry much more current than their on-chip counterparts. This larger current would induce crosstalk primarily in a magnetic or inductive mode, (as opposed to a capacitive mode). Generally, with multi-Gbps data-rate trends, link designs warrant careful considerations on reflections at impedance transitions (for example, where traces change levels at vias), lest crosstalk noise will be induced by densely packed neighboring connections; and high-frequency attenuation due to skin effect (in metal traces) and dielectric losses will also concurrently prevail. Further at muti-Gbps bitrates, the bit duration is invariably shorter than the flight-time along interconnects; as such, echoes of previous pulses may arrive at the receiver on top of the original pulse (and corrupt it thereof). This amounts to *intersymbol interference* (ISI) viewed in SI engineering as “eye closure” (depicting the clutter in the center of a CRO trace of an eye diagram).

Illustrated in Figure 1 is the context of a clock and a data signal. The data signal latches at the rising edge of the clock. *Set up time* indicated is the amount of time before the clock edge that the input signal needs to be stable so it has a guarantee of being accepted properly on the clock edge. *Hold time* denotes the amount of time after the clock edge that same input signal has to be held before changing it in order to make sure that it is sensed properly at the clock edge.

Set up and hold times are crucial in chip design to ensure that they meet the application specifications. Therefore, they should not deteriorate when the clock/signal pulses traverse along the PCB traces/interconnects. Should any change occur in setup and/or hold times during the transit of signal/clock pulses, logic upsets may occur due to edge rate violations. For example, assuming a clock rate of 1 MHz with slow edge rate, a setup time violation may not be invoked. However, for 1 GHz clock (and fast edge rates), the bus-technology and the setup time requirements of the destination IC should be carefully designed for SI.

Though SI engineering is normally conceived to address digital format of signals at any locale of the system, in modern context, its implications are critically severe at the logic-gate sites in the circuits of a VLSI/ULSI system. More so, the scaling trends in VLSI/ULSI implementations in recent times warrant channel sizes of MOS-technology below 0.25 μm. Corresponding wire-

transit delays have become comparable or even greater than the gate delays. Further, in nanometer technologies at 0.13 μm and below, unintended interactions between signals (or noise) becomes a crucial issue in digital designs. At these technology-nodes, the performance and correctness of a design cannot be assured without due considerations of noise effects implicating the signal integrity. Relevant issues can be summarized as:

- SI-specific noise may cause a signal to assume a wrong value. This is critical when the signal is about to be latched, for a wrong value can be loaded into a storage element.
- SI-specific noise may also delay the settling of the signal to the correct value. This is often referred to as *noise-on-delay*.
- SI-specific noise may lead to the input voltage of a gate to go below ground, or to exceed the supply voltage. This does not affect correct operation but may reduce the lifetime of the device.

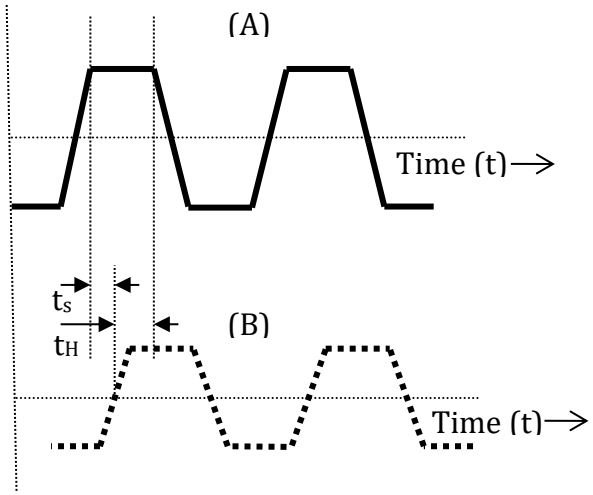

Fig.1: Digital waveform (A) compared with a reference clock-pulse (B). (t_s: Setup time; and t_H: Hold time)

In short, in conceiving modern SI engineering, the primary focus has been the CMOS technology scaling into the deep sub-micrometer regime. Here, digital noise is becoming a metric of importance comparable to area, timing, and power in the analysis and design of CMOS VLSI systems. As mentioned above, relevant SI-specific noise can destroy logical information carried by a circuit net. Also, it may cause delay uncertainty: That is, even non-critical paths might become critical because of noise. As such, circuit speed becomes limited by noise, primarily due to capacitive EM coupling between wires/traces. Largely, crosstalk noise issues are addressed at the layout generation stage, or *via* post-layout corrections. However, with the advent of continued scaling, number of circuit nets that require corrections for noise becomes unmanageably large causing a design convergence problem.

In summary, SI engineering has been a comprehensive art to understand the digital waveform impairments and consequent circuit performance involving high-density traces on PCB, chip-to-chip lines, on-chip lines etc. Aggravated situations with scaled-down VLSI/ULSI implementations in CMOS devices of sub-quarter micron technology plus multi-Gbps data

transfers have brought the traditionally defined framework of SI engineering to the pinnacle of its importance in recent times.

SIGNAL INTEGRITY – A GLOBAL PERSPECTIVE

Apart from the exclusive domain of (baseband) digital signals, the authors extend here the definition of signal integrity to RF stages and situations in an electronic circuit or systems by including relevant electromagnetics and transmission-line parasitic aspects that may influence the signal integrity at large. Relevant perspective explores whether SI considerations are warranted at RF stages of modern wireless systems (such as in IEEE 802.11 devices) and if so, plausible logistics are analyzed.

Further, notwithstanding the traditional (baseband) waveform impairments in digital waveforms indicated before and suggested possible artifacts due to RF-stage electromagnetics, the prevailing scope of SI engineering also includes signal waveform profiling under power transients, ESD/EoS effects and ionizing radiation stresses. In short, a global perspective on SI engineering issue refers to: (i) the base of digital infrastructure of modern VLSI/ULSI and PCB systems, (ii) inevitable noise encroachments on the signal, (iii) RF-stage electromagnetic (EM) implications on signal integrity, (iv) undesirable influences due to power-transients, (v) possible ESD/EoS effects and (vi) (space-ambient) ionizing radiation stresses. Among these, the specific aspects of EM/transmission-line considerations at RF-stages (of wireless circuits) are addressed in this paper to formulate the etiology and reasons for the associated SI concerns.

Artifacts in RF-modulated Waveforms in Pre-detection Stages

Consider a modulated RF signal in the pre-detection stage(s) of a system. It is of interest to identify first possible artifacts in the RF signal waveform that may incur due to the associated transmission-line effects and other parasitic considerations. Essentially, the RF sinusoid would experience possible (transit) delays (caused by reactive transmission-line plus parasitic parameters) as well as may get attenuated due to line losses.

The time-offsets observed in the RF pulse is presumed to be the result of, for example, delay (τ_{RF}) experienced by a sinusoidal RF signal due to its transit from an originating device (D_1) and a termination device (D_2) as illustrated in Figure 2 where (i) depicts the RF signal at the origin and (ii) refers to its format at the terminal device. Not only does the RF signal experience a delay (τ_{RF}) across the transit path, it may also suffer attenuation in its original amplitude a, reducing to b < a (due to line-losses). It is contended here that any waveform-related deteriorations in signal characteristics should be considered as an SI issue. For example, attenuation in an RF-signal waveform (due to signal transit-path) implicates further processing value of the signal (expressed in signal-to-noise ratio, SNR) in subsequent stages of the circuit. That is, should an RF- signal be impaired because of transit from one stage to the other or otherwise, the resulting damped- SNR will hamper ensuring signal quality toward processing in the circuit blocks ahead.

This situation is illustrated in the following section with a practical example *via* transit-path induced transmission-line parasites that may affect the design-performance of transmit-receive (TR) switch designed for inclusion in a Bluetooth transceiver [6]. Relevant RF- specific

issues at the transceive path between the antenna and active TR-switch CMOS configuration in causing SI concerns are evaluated and discussed.

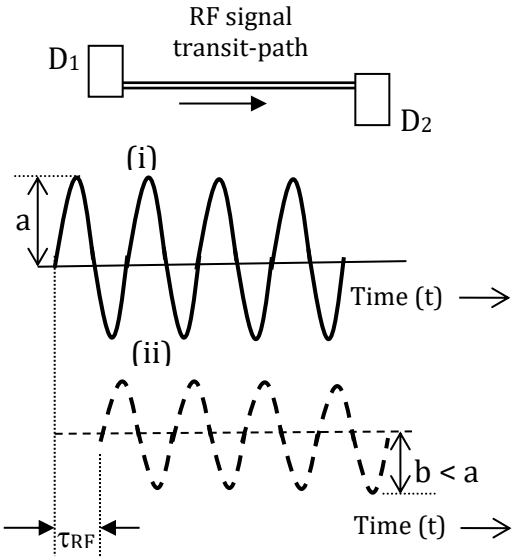

Fig. 2: (i) RF signal at the origin (D_1); and (ii) format of the RF signal at the terminal device (D_2) after its transit along a certain path. (τ_{RF}: Transit delay experienced by the RF sinusoid)

RF-LEVEL SI ISSUES: EXAMPLE

The SI considerations at RF level can be illustrated with reference to a typical RF stage, for example, the transmit/receive (TR) switch (in the transceiver) of a wireless radio (such as a Bluetooth). This switch directs the outgoing transmitter signals to the antenna as well as brings the incoming signals (received at the same antenna) to the receiver. That is, the TR-switch is intended to accomplish necessary segregation of transceive signals to facilitate selective bifurcation of transmit and receive paths for the RF signal at the front/back-end (at the antenna section).

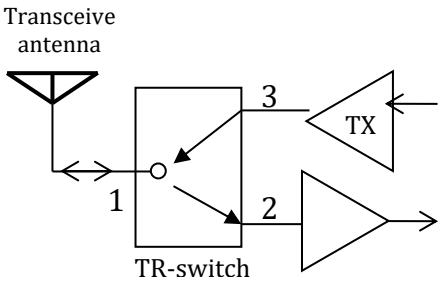

Fig. 3: Concept of TR switching. (Tx: Transmitter. Rx: Receiver)

Considering the TR-switch function as above, the main design factors of interest in specifying the RF signal integrity are: (a) *Insertion loss* (IL); (b) *isolation* (IS) and (c) *noise factor* (NF). These performance features on a test circuit can be analyzed using simulation tools (such as the S-parameters simulation tool in ADS™) and they can be defined with reference to Figure 3

[6]. In Figure 3, termination 1 is the antenna-port, termination 2 is the receive-port and termination 3 is the transmit-port, which are all 50 ohms impedance. The TR-switch toggles transmit and receive mode signals between the terminations 1, 2, and 3 as appropriate.

The TR-switching facilitated by a compatible RF CMOS-VLSI configuration, foe example is illustrated in Figure 4. It is a typical topology [6] used in Bluetooth-radios. When the transistor for the transmit path (in Figure 4) is turned ON and the transistor in the receive path is turned OFF, the ratio of output power from port 3 to input power at port 1 is the measurement of the switch *insertion loss* (IL) specified as a S-parameter, S_{31}. When the receive path is turned ON and the transmit path is turned OFF, the ratio of output power at port 3 to input power at port 2 is the measurement of the switch *isolation* (IS) denoted by S-parameter, S_{32}. Further, the *noise figure* (NF) refers to the measure of degradation of the signal-to-noise ratio (SNR), caused by any block/section in the RF signal chain, (which in the present context is the TR switch).

NF refers to the ratio of the output noise power of a device (or circuit block in question) taken to the portion thereof attributable to the device (circuit block) thermal noise in the input termination (normally specified at standard noise temperature T_o (namely, 290^o K). Thus, NF in essence defines the ratio of actual output noise to that which would remain if the device (circuit block) itself did not introduce noise. With reference to Figure 4, the NF specified at port 3 when the switch is in the transmit mode.

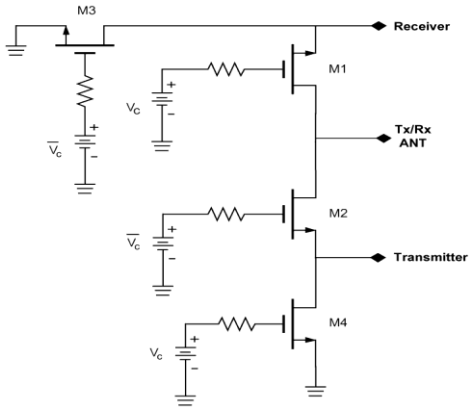

Fig. 4: A TR-switch using CMOS technology.

Typical design and performance issues involve ascertaining the insertion loss, isolation and noise figure when the transmitter side is active. Therefore, IL is determined from the antenna to the transmit path, where it is measured as a ratio of output power at the transmitter load to input power from the antenna. IS is determined from transmitter to receiver path, where it is measured as a ratio of output power at the transmitter load to input power from the receiver.

TR- Switch: Expected Performance *vis-à-vis* Signal Integrity

As mentioned before, the transmit/receive switch in question should provide selective bifurcated isolation of transmit and receive paths for the RF signal at the antenna section. As such, the insertion loss (IL/S_{31}), isolation (IS/S_{32}) and noise factor (NF) are essential design

concerns and performance indices towards exercising SI in an RF transmit/receive switch design and implementation. Presently, such parameters of SI interest are evaluated in a test Bluetooth circuit using S-parameters simulation tool in ADS™.

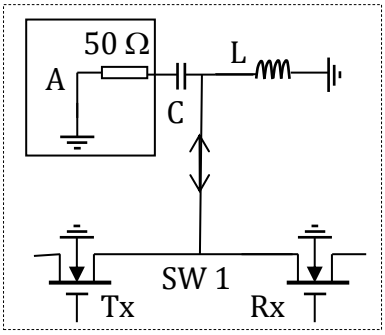

Fig. 5: Bench-mark circuit with {L, C}: Designed topology of TR switch for a Bluetooth transceive circuit. (A: Antenna section and {L, C} denotes optimized lumped LC-elements obtained from the design).

In facilitating the transit of to-and-fro RF signal between the antenna, the topology of Figure 5 (depicting a benchmark circuit) is optimized with {L, C} in the design to achieve the "best" isolation (IS), minimum attenuation (insertion loss, IS) and for minimum noise figure (NF). However, in fabrication, should any parasites be introduced at this (L, C) section, then the signal transit-path between antenna-to-CMOS devices can be modeled by a variety of resonant/filter configurations illustrated in Figures 6-1 to 6-12 (and marked as SW 2 to SW 13). (In Figures 6-5 through 6-12, the designed values of the set {L, C} are different and indicated as {L′, C′}. Further, the parasite-infested region in each circuit of Figures 6-1 to 6-12 is shown with grey-shading.

First, simulations are performed with the designed section of the TR-switch of a Bluetooth transceiver configuration illustrated in Figure 5 and marked as SW 1. It is a design-optimized benchmark circuit where the antenna (simulated as a 50 □ resistance) is shown as the block, A; and {L and C} denotes a set of designed values introduced as lumped elements in the circuit in order to couple the antenna to the active (CMOS-based) TR-switching architecture that emulates the segregated paths of transmitter (Tx)-to-antenna and antenna-to-receiver (Rx).

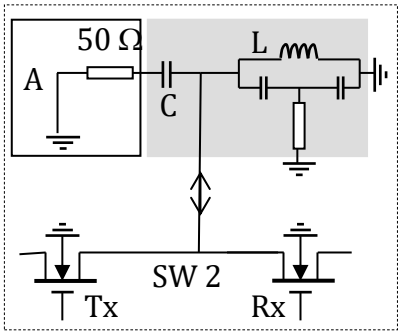

Fig. 6-1: SW 2- Parasite-infestation emulating Colpitts resonance at L

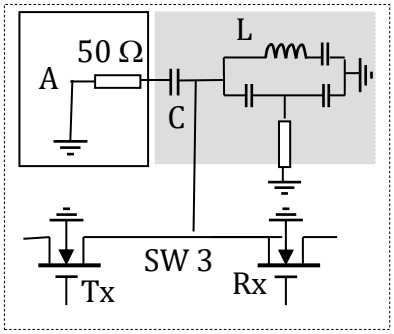

Fig. 6-2 SW 3 - Parasite-infestation emulating Clapp resonance at L

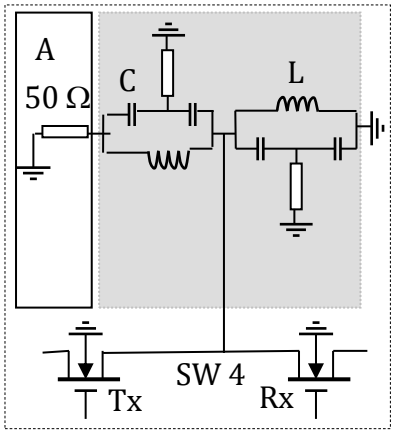

Fig. 6-3 SW 4 - Parasite-infestation emulating Colpitts resonance both at L and C

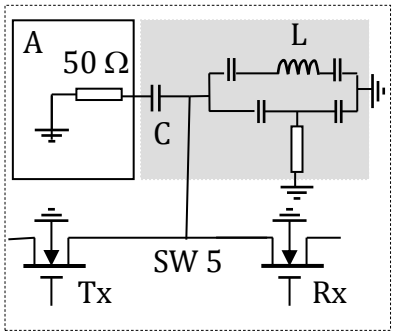

Fig. 6-4 SW 5 - Parasite-infestation emulating Seiler resonance at L

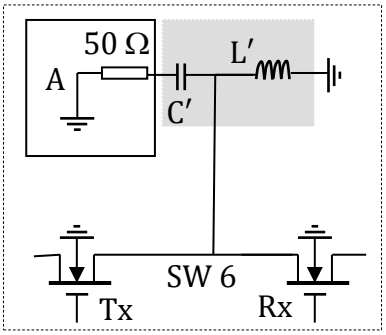

Fig. 6-5 SW 6 - Bench-mark circuit with {L, C} modified to {L′, C′}

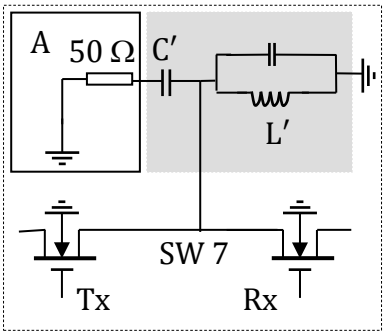

Fig. 6-6 SW 7 - Parasite-infestation emulating parallel resonance at L′

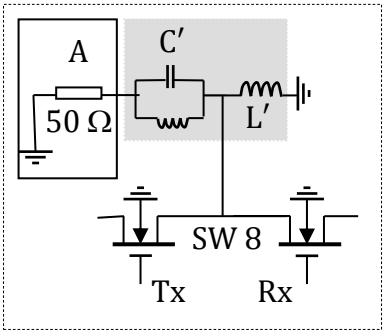

Fig. 6-7 SW 8 - Parasite-infestation emulating parallel resonance at C′

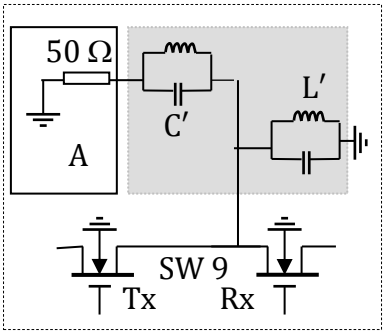

Fig. 6-8 SW 9 - Parasite-infestation emulating parallel resonance at L′ and C′

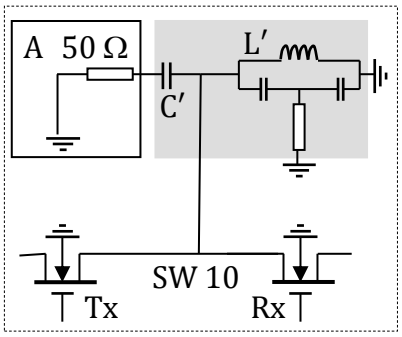

Fig. 6-9 SW 10 - Parasite-infestation emulating Colpitts resonance at L′

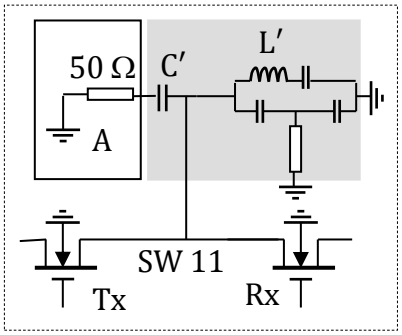

Fig. 6-10 SW 11 - Parasite-infestation emulating Clapp resonance at L′

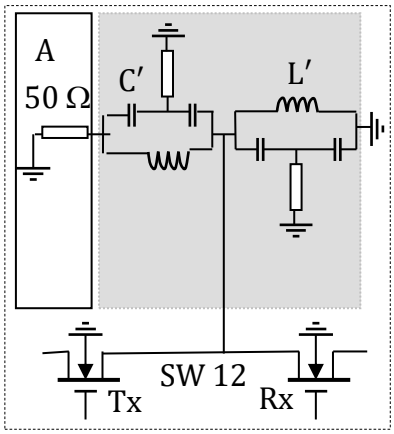

Fig. 6-11 SW 12 - Parasite-infestation emulating Colpitts resonance at L′ and C′

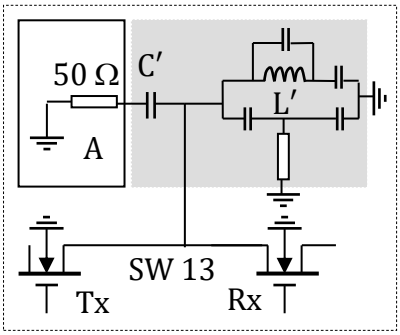

Fig. 6-12 SW 13 - Parasite-infestation emulating Seiler resonance at L′

In summary, Figures 6-1 to 6-12 represent a hypothetical set of designed TR-switch topology compatible for a Bluetooth transceive circuit but, from the antenna section (A) through the designed (L, C) or (L′, C′) section (depicting the RF signal to-and-fro transit-path), hypothetical capacitive and inductive elements are introduced (shown grey-shaded) so as to emulate parasitic resonance/filtering influences on RF signal. The presence of such parasites will impair the RF-signal transceive performance evaluated in terms of IL, IS and NF parameters specified earlier. In the present study, the performance of parasite-infested test circuits *versus* that of the benchmark design (Figure 5) is evaluated using ADS™ simulation. The test TR-switch circuit corresponds to a Bluetooth receiver design with RF CMOS-VLSI devices described in [6].

SIMULATION RESULTS

As mentioned above, the computed results on the three SI performance indicators, namely, IL, IS and NF (obtained *via* ADS™ tool) for the test circuits of Figure 5 and Figures 6-1 to 6-12 are tabulated in Table 1; and Bluetooth-implied design parameters adopted in ADS™ simulations are presented in Table2.

Table 1: ADS™ simulation results on IL, IS and NF for the bench circuit (Figure 5) and different versions of parasite-infested configurations (of Figures 6-1 to 6-12)

SW #	IL in dB	IS in dB	NF in dB
SW1	– 7.780	– 70.487	7.314
SW 2	– 9.204	–71.911	8.976
SW 3	– 68.881	–131.59	68.310
SW 4	– 22.631	–64.168	22.397
SW 5	– 71.074	–131.60	70.500
SW 6	– 6.1260	– 66.648	5.8590
SW 7	– 9.1410	– 69.664	8.9770
SW 8	– 25.800	– 67.794	24.900
SW 9	– 20.376	– 62.368	20.093
SW10	– 10.196	– 70.719	10.002
SW11	– 10.312	– 70.834	10.118
SW12	– 26.300	– 64.880	26.105
SW13	– 16.995	– 77.518	16.597

Table 2: Bluetooth-implied design parameters adopted in ADS™ simulations

Emulated Circuit Design Details [6]:
Bluetooth operation at ISM RF carrier frequency: 2450 MHz Antenna impedance: 50 Ω Matching characteristic impedance(s): 50 Ω Terminal impedances: 50 Ω CMOS process parameters correspond to: CMOS process of Taiwan Semiconductor Company (TSMC) 0.35 micron process: (CM035 TSMC35_PL) and the PSPICE parameters for this process is based on BSIM3v3.1 (Berkeley Short-Channel IGFET Model equations. Operating voltage: 3.3 volt

CONCLUSIONS

From Table 1, it can be observed that significant variations in the SI parameters of interest are caused by various parasitic influences emulated. These parameters also mutually affect each other. Typically, a reduction in IL causes a reduction in IS and NF; and an increase in IS causes an increase on IL and NF.

Therefore, once the performance is optimized towards realizing a benchmark setup, unless care is taken in the fabrication of the RF section parasites will be introduced. As such, the RF-level signal integrity will be impaired. Hence to conclude:

- RF level SI awareness is necessary.
- SI parameters at RF level can be specified by the S-parameters of the block of interest. (Presently, relevant S-parameters refer to IL, IS, and NF)
- Simulation tools such as ADS™ are helpful in identifying possible parasitic and other malicious influences on signal integrity.
- Simulations result with split-inductor resonance configurations (Hartley resonance circuit) emulating the parasites at (L, C) or (L′, C′) are not shown in this paper. Again, relevant details also indicate adverse effects on SI at the RF stage under discussion.

In all, the hardware performance of smart handheld devices relevant to RF section; and PCB transports across dense traces in addition would require rigorous analytic suites to indicate mitigation strategies towards achieving high signal integrity as outlined in [6]-[8].

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