AIVP ADVANCES IN IMAGE AND VIDEO PROCESSING
SOCIETY FOR SCIENCE AND EDUCATION UNITED KINGDOM
VOLUME 3, ISSUE 1
ISSN: 2054-7412

A 100 MHz 6th Order Continuous Time Band-Pass Sigma Delta Modulator with Active Inductor based Resonators

[1]Kevin Dobson, [2]Shahrokh Ahmadi and [3]Mona Zaghloul
Department of Electrical and Computer Engineering, George Washington University, Washington DC, USA;
[1]kdobson@gwu.edu, [2]ahmadi@gwu.edu, [3]zaghloul@gwu.edu

ABSTRACT

This paper presents a 6th order, continuous time band-pass Sigma Delta modulator in IBM 0.18 um CMOS technology. We replace traditional RLC circuits, containing low quality factor spiral inductors with high quality factor, active inductor based resonators utilizing negative impedance circuits. Pad to pad simulation of the extracted layout in Cadence yields an enhanced SNDR of 78 dB with a noise bandwidth of 18 kHz and a power consumption of 12 mW. Our modulator occupies 7.5 mm^2 of chip area with pads.

Keywords: Sigma Delta; Active Inductor; Negative Impedance circuit.

1 Continuous Time Sigma Delta Modulator Loop Filter

In Figure-1 below we see the block diagram of a Continuous Time Sigma Delta (CT ΣΔ) modulator. In order to design the loop filter *G(s)* we start with a discrete time modulator transfer function *F(z)* which provides the required noise shaping.

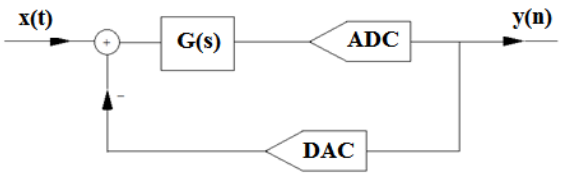

Figure-1: Continuous Time Sigma Delta Modulator

As outlined in [1], the impulse-invariant method is used to generate the equivalent CT loop filter *G(s)* from *F(z)*.

$$F(z) = (1 - z^{-1}) Z_T \{ L^{-1} [\frac{G(s) e^{-ds}}{s}] \} \tag{1}$$

Here *d* represents the delay introduced by the Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC). For a sixth order band-pass Sigma Delta modulator, the equivalent continuous time loop filter transfer function is given by:

$$G(s) = \frac{(s-p)(s^2 + \frac{\omega_a}{Qa} s + \omega_a{}^2)(s^2 + \frac{\omega_b}{Qb} s + \omega_b{}^2)}{(s^2 + \frac{\omega_0}{Q_0} s + \omega_0{}^2)(s^2 + \frac{\omega_1}{Q_1} s + \omega_1{}^2)(s^2 + \frac{\omega_2}{Q_2} s + \omega_2{}^2)} \tag{2}$$

DOI: 10.14738/aivp.31.999
Publication Date: 22nd February, 2015
URL: http://dx.doi.org/10.14738/aivp.31.999

ω represents the normalized resonator frequencies with respect to the sampling frequency in radians per second and Q is the quality factor of the resonators. If we denote T as the sampling frequency, when d is equal to 1.4T and the sample rate is 4 times the frequency of the input signal, then the term p in the numerator is approximately equal to zero [2].

2 Active Inductor Resonator structure

The transfer-function of a parallel RLC resonator circuit $H(s)$ is given by:

$$H(s) = \frac{As}{s^2 + \frac{\omega_0}{Q} + \omega_0^{\ 2}} \tag{3}$$

$G(s)$ cannot be realized as a cascade of resonators but can be realized by the structure shown in Figure 2 which appropriately places the poles and zeros. Here g, A_H and A_L represent amplifier gains, and H the resonators. The Σ block is an analog adder. H_0, H_1 and H_2 are high Q resonators and provide noise shaping. H_3 is a low Q resonator which provides modulator stability.

A review of the available literature will show that most band-pass CT ΣΔ modulators have a loop filter containing parallel RLC circuits with spiral inductors. Such circuits occupy a large silicon area and the spiral inductors have a low Q. Active inductor based resonator circuits occupy a much smaller area leading to more economical designs. When Q enhancement techniques are used, high Q can be achieved. Active inductor based resonators are explained by the gyrator C theorem as outlined in Figure iii below.

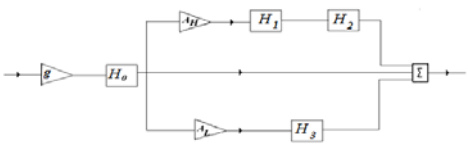

Figure 2: Sixth Order Loop Filter

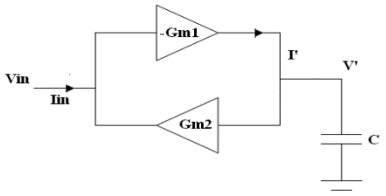

Figure 3: Gyrator Topology

It is easily shown that:

$$\frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}} \tag{4}$$

The s in the numerator of Eq. (4) indicates the inductive nature of the circuit. When MOSFETs are used to realize G_{m1} and G_{m2} additional parasitics are introduced forming a lossy parallel RLC resonator circuit as shown in Figure 4 below.

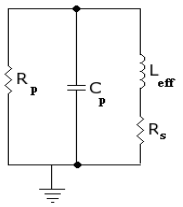

Figure 4: Lossy Parallel RLC Resonator

Copyright © Society for Science and Education United Kingdom

When two such gyrators are coupled with a Negative Impedance Circuit (NIC), as shown in Figure v, a high *Q* fully differential resonator, for use in a band-pass ΣΔ modulator, can be designed.

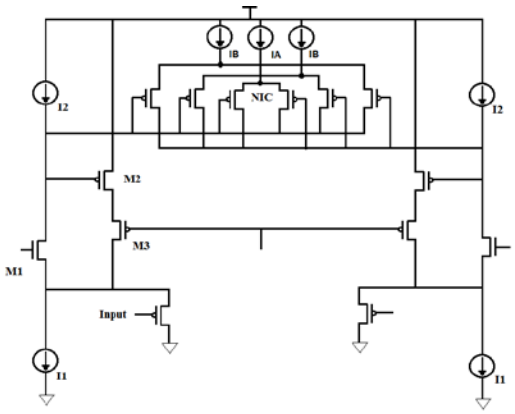

Figure 5: CMOS Active Inductor based Resonator with NIC

Upon performing a small signal analysis of the circuit in Figure v and separating the resistive, capacitive and inductive parts we get the following equations [3]. g_o is the drain source conductance and g_m the transistor transconductance. C_{nic} represents the additional capacitance introduced by the NIC and g_{nic} its transconductance.

$$R_p = \frac{1}{g_{o2}};\ C_p = C_{gs1};\ L_{eff} = \frac{C_{gs2}}{g_{m1}g_{m2}};\ \text{and}\ R_s = \frac{g_{o1}g_{o3}}{g_{m1}g_{m2}g_{m3}} \tag{5}$$

The enhanced self-resonant frequency and quality factor of the circuit is given respectively by:

$$\omega_{en} = \sqrt{\frac{C_p}{C_p + C_{nic}}}\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \tag{6}$$

$$Q_{en} = \frac{1}{g_{o2} - g_{nic}}\sqrt{\frac{C_p + C_{nic}}{L_{eff}}} \tag{7}$$

PMOS devices are used to couple the differential input to the circuit. They are biased to draw a small amount of current and do not disturb the gyrator function. Output gain is controlled by varying the size of these PMOS devices. Cascoding M3 and M2 reduces the output conductance which reduces R_s and increases the *Q*.

The NIC is comprised of 3 cross-coupled differential pairs of PMOS devices with drains tied to the opposing gates. It provides a negative resistance that attempts to cancel the parallel resistance R_p which further increases the *Q*. The use of PMOS devices allows for current reuse and results in less power consumption. Single pair cross-coupled NICs exhibit low linearity [4]. In order to obtain greater linearity a multi-tanh version of the NIC circuit is used. This requires the addition of two extra cross-coupled pairs of MOSFETs with a 4:1 size ratio [5][7]. When the signal is large and the symmetrical differential pair has saturated, the unbalanced differential pairs can still provide a differential current proportional to the input voltage. This scheme works effectively at high frequencies.

While there are no limits to the voltage that can be applied to spiral inductors, the maximum input voltage to active inductor based circuits cannot cause MOSFETs to cease operating in saturation mode. Active inductor based circuits are also noisier than circuits with real inductors by a factor of $2Q_0$, the intrinsic quality factor [5]. All current sources used are cascode in order to provide greater linearity.

3 Active Inductor Simulation

We were able to design and simulate active inductor based resonators in Cadence with resonant frequencies between 15 MHz and 1.5 GHz, and were consistently able to achieve a Q of 50 or greater. Simulation results for one active inductor designed are shown in Figure 6 and 7.

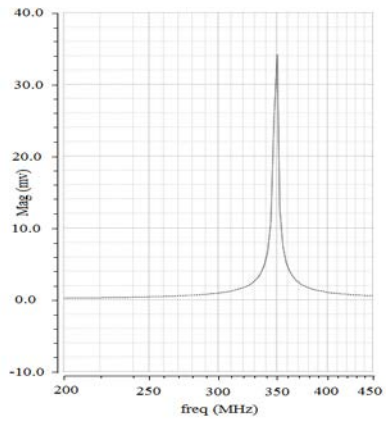

Figure 6: Active Inductor simulated AC response

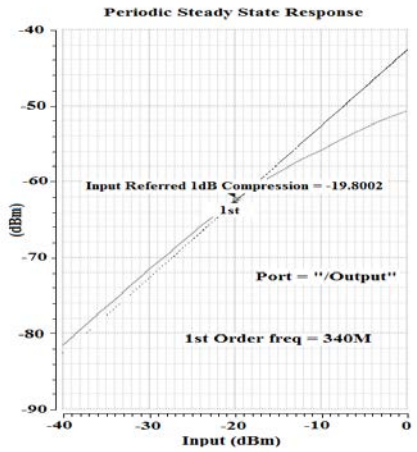

Figure 7: Active Inductor Linearity

4 Matlab Modulator Simulation

Initial values of the loop filter multiplying coefficients g, A_H and A_L of $G(s)$ were used to generate Pole-Zero plots and confirm modulator stability. The appropriate noise shaping characteristics were verified by the use of the Delta-Sigma toolbox [6]. Simulink simulations were then used to further refine the modulator design.

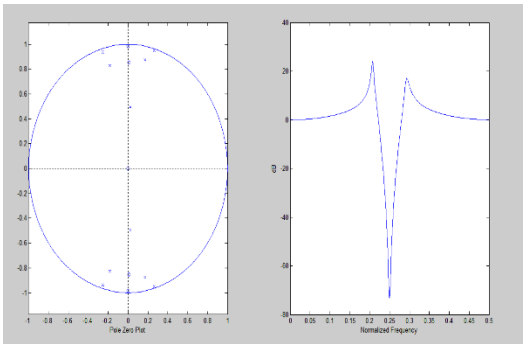

Figure 8: Modulator Pole Zero plot

The Simulink model was easily modified to reflect the non-idealities of an actual circuit such as limited gain due to nonlinearity and small delays introduced by each circuit component. A theoretical Signal to Noise-plus-Distortion Ratio (SNDR) of 95dB was obtained for the ideal case when there is a high gain in the path containing the most resonators. When the limitations of gain and circuit delay were taken into account a goal of 80 dB was deemed feasible.

Copyright © Society for Science and Education United Kingdom

5 Cadence Simulation

For the Cadence circuit design, resonators were designed to resonate at 25 MHz with a *Q* of 30. Linear operation was observed when the input was limited to less than 10mv p-p. A block diagram of the complete circuit simulated in Cadence is shown in Figure ix.

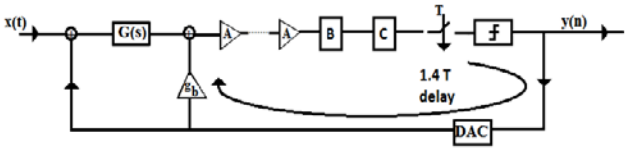

Figure 9: Active Inductor based Sixth Order Continuous Time Modulator

A series of differential amplifiers[8] *A*, provide effective amplification of the signal prior to quantization preventing clock feed-through [8] and contributing to the required delay of 1.4T. A coupling capacitor with buffer for biasing the next stage of the circuit, B, eliminates dc offsets introduced after layout. This capacitor and input resistance of the buffer must be large enough to form an effective high pass filter thereby preventing attenuation. Pre-comparators C provide further amplification before quantization by a clocked comparator. Since there is a non-zero delay it is necessary to add a direct loop between the DAC and the ADC input [9]. The Adder used is described in [2]. A 2 input version of the adder is used to subtract the DAC output from the input signal. Conceptually the subtraction is the addition of the input and the negative DAC output. A clocked comparator [8] coupled with a SR flip flop generates the (NRZ) modulator output. The DAC is described in [10].

We use separate VDD and GND for these sub-circuits. We also surround our analog sub-circuits with two guard rings separated by BFMOAT in order to protect them from digital noise. [11]

Extraction of the layout yields extra parasitics which result in larger propagation delays and lower output signals, resonant frequency and *Q*. Several circuit modifications were made in order to negate the effects of the added parasitics. The first was to ensure a symmetrical layout so that the parasitics added on either side of the differential circuit were equivalent. The next was to increase the size of the input PMOS devices leading to better coupling of input signals. The third was to increase the current in the current mirror I2 which is necessary to overcome the added impedances. The fourth was to increase the size of M3. This decreases R_s which increases our deteriorated *Q*. The fifth was to lower our clock frequency to account for the increased propagation delays. When these changes were made to the layout and Input/ Output pads added, the layout was re-extracted and a pad to pad simulation was conducted.

This yielded a SNDR of 78dB with a noise bandwidth of 12 kHz. This was quite close to the 80dB observed in the Simulink simulations. The difference is believed to be due to circuit non-idealities, such as settling time of the adder output, and offset errors. This result is shown in Figure 10. It compares favorably with other non-active inductor based sixth order band-pass ΣΔ modulators such as [12], which yields a SNDR of 68dB. Our circuit consumes 12 mW and occupies 7.5 mm^2, including pads.

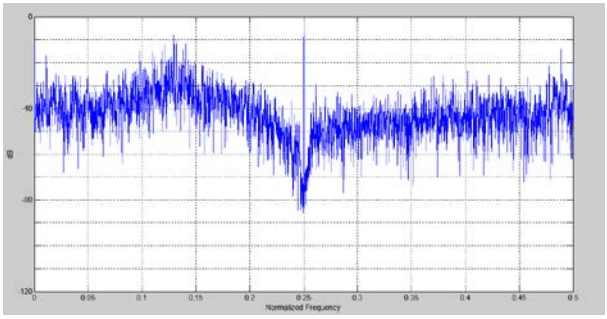

Figure 10: Extracted Layout Power Spectrum Density

6 Conclusion

The greatest design limitation encountered when designing CT ΣΔ modulators with active inductor based resonators is the limited linearity. This results in a design that is highly susceptible to offsets. Also many extra amplification stages are necessary to raise voltages to acceptable levels prior to quantization. The extra circuitry required to compensate for offsets and amplification negates the area gains made by the avoidance of spiral inductors. More research is needed to determine how to extend the linearity of active inductor based resonators. This would result in designs that are capable of operating at higher frequencies and occupying smaller areas.

A review of the available literature shows only one other active inductor based band-pass ΣΔ modulator [13]. The authors included schematic simulations but not simulation results for an extracted layout. We have succeeded in designing and simulating the first Sixth Order CT ΣΔ modulator, using active inductor based resonators in the loop filter and provided pad to pad simulations of the extracted layout. Our design has been submitted for fabrication with MOSIS.

REFERENCES

[1] C. Lelandais-Perrault, P. Benabes, J. De Gouy, R. Kielbasa, *A parallel structure of a continuous-time filter for bandpass sigma-delta A/D Converters*, 10th IEEE International Conference on Electronics, Sharjah (Emirates Arabes Unis), DEC. 2003.

[2] S. Benabid, P. Benabes, *High linear integrated LC filter for a continuous-time bandpass sigma-delta ADC* Circuits and Systems, 2003 IEEE 46th Midwest Symposium on, pp. 291 - 294 Vol. 1, 30 Dec. 2003

[3] Fei Yuan, *CMOS Active Inductors and Transformers, Principle, Implementation, and Applications*, Springer 2008

[4] Byunghoo Jung, Harjani, R., *A wide tuning range VCO using capacitive source degeneration,* Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on, Volume 4, 23-26 May 2004, Page(s): IV - 145-8 Vol.4.

[5] Yue Wu, Xiaohui Ding, Mohammed Ismail, and Håkan Olsson, *RF bandpass filter design based on CMOS active inductors*, IEEE Transactions on circuits and systems—II: Analog and Digital Signal Processing, vol 50, no.12, Dec. 2003.

[6] Richard Schreier and Gabor C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press

Copyright © Society for Science and Education United Kingdom

[7] A. P. Ryan, O. McCarthy, *A novel pole-zero compensation scheme using unbalanced differential pairs*, IEEE transactions on circuits and systems—I: Regular papers, vol. 51, no. 2, Feb. 2004.

[8] R. Jacob Baker, *CMOS, Circuit Design, Layout, and Simulation*, IEEE Press Series on Microelectronic Systems.

[9] P. Benabes, M. Keramat and R. Kielbasa, *Synthesis and Analysis of Sigma-Delta Modulators Employing Continuous-Time Filters*, Analog Integrated Circuits and Signal Processing, no. 23, pp. 141-152, Jul. 1998.

[10] Kevin Dobson, Shahrokh Ahmadi and Mona Zaghloul, *A 1.2 GHz Band-Pass Sigma Delta Analog to Digital Modulator with Active Inductor based Resonators*, Lecture Notes in Engineering and Computer Science: Proceedings of The World Congress on Engineering and Computer Science 2012, WCECS 2012, 24-26 October, 2012, San Francisco, USA, pp 875-879

[11] Haitao Dai, *Differential Sensing of Substrate Noise in Mixed-Signal 0.18- um BiCMOS Technology*, Electron Device Letters, IEEE, Aug. 2008, Volume 29: Issue 8, pp 898-901

[12] Cho-Ying Lu, Silva-Rivas, J.F.; Kode, P.; Silva-Martinez, J.; Hoyos, S., A Sixth-Order 200 MHz IF Bandpass Sigma-Delta Modulator With Over 68 dB SNDR in 10 MHz Bandwidth, Solid-State Circuits, IEEE Journal of, Volume: 45, Issue: 6, 2010 , Page(s): 1122 – 1136

[13] Quining Chen, Kamal El-Sankary and Ezz El-Masry, *A UHF continuous-time current-mode band-pass delta sigma modulator based on active inductor*, Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on